A 195-Gb/s 1.2-W Inductive Inter-Chip Wireless Superconnect With Transmit Power Control Scheme for 3-D-Stacked System in a Package

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***Abstract*—A wireless interface by inductive coupling achieves aggregated data rate of 195 Gb/s with power dissipation of 1.2 W among 4-stacked chips in a package where 195 transceivers with the data rate of 1 Gb/s/channel are arranged in 50-μm pitch in 0.25-μm CMOS technology. By thinning chip thickness to 10 μm, the interface communicates at distance of 15 μm at minimum and 43 μm at maximum. A low-power single-end transmitter achieves 55% power reduction for multiple connections. The transmit power is dynamically controlled in accordance with communication distance to reduce not only power dissipation but also crosstalk.**

***Index Terms*—High bandwidth, inductor, low power, SiP, three-dimensional, wireless interconnect.**

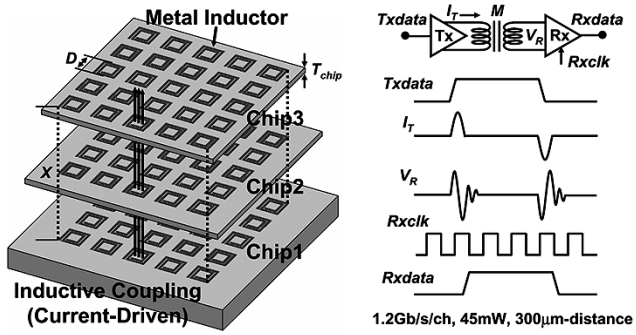

Fig. 1. Inductive inter-chip wireless superconnect (WSC).

I. Introduction

LSI SYSTEMS require high-bandwidth interfaces to close the increasing performance gap between computations in a chip and communications between chips. Serial link techniques in System-on-a-Board (SoB) implementation reaches 40-Gb/s operation [1], [2]. However, the long inter-chip distance in SoB requires high power dissipation (>3 W) and large area (>20 mm^2) for circuits which limits the number of connections and bandwidth. On-chip network [3], [4] in System-on-a-Chip (SoC) technology is one of the solutions to meet the demand. However, cost increase due to a complex embedded process is the problem of SoC. Three-dimensional (3-D) interfaces in System-in-a-Package (SiP) solve the problem. Functions embedded in the system, such as CPU and memory, can be separately designed and fabricated in a standard fabrication process which is optimized for each function. On top of that, SiP reduces distance between chips significantly (<100 μm) in its 3-D-stacked structure, enabling high-speed, high-density and low-power 3-D interfaces.

Three-dimensional interfaces are classified into two groups: wired and wireless approaches. In wired approaches, like micro-bump [5], [17], [18] and through-silicon-via (TSV) [6] technologies, issues are cost increase caused by an additional mechanical process and yield degradation due to difficulty in screening a known good die (KGD) since the wired interface cannot be tested at high operating frequency before assembly. On the other hand, wireless approaches utilizing inductive and capacitive coupling [7]–[12] are circuit solutions where the interface, a metal inductor for inductive coupling and a metal plate for capacitive coupling, can be implemented in a standard LSI process without the additional mechanical process, which allows significant cost reduction, high scalability by exploiting process scaling, and high reliability. Since the wireless interface is a noncontact interface, it can remove highly capacitive electrostatic discharge (ESD) protection devices. The absence of ESD protection, high-pass filtering property, and detachability of the noncontact interface allows at-speed testing before assembly, solving the KGD problem [13].

The inductive coupled wireless interface [7]–[9] has several advantages over the capacitive coupled wireless interface [10]–[12]. Since capacitive coupling is a voltage-driven scheme, it cannot increase transmit power at low supply voltages in current scaled devices, and as a result, capacitive coupling can be employed only when two chips are stacked face-to-face. On the other hand, inductive coupling is a current-driven scheme, so transmit power can be increased even at low supply voltages in scaled devices which enables more than three-stacked inter-chip communications whether chips are stacked face-up or face-down. Therefore, in addition to the multi-drop bus connections, the interface can be applied when a lower chip is mounted on an area-bump package or an upper chip has imaging sensors. Power and ground can be easily provided by bonding wires or area bumps without the micro-bump or

Manuscript received April 5, 2005; revised July 8, 2005.

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Digital Object Identifier 10.1109/JSSC.2005.858625

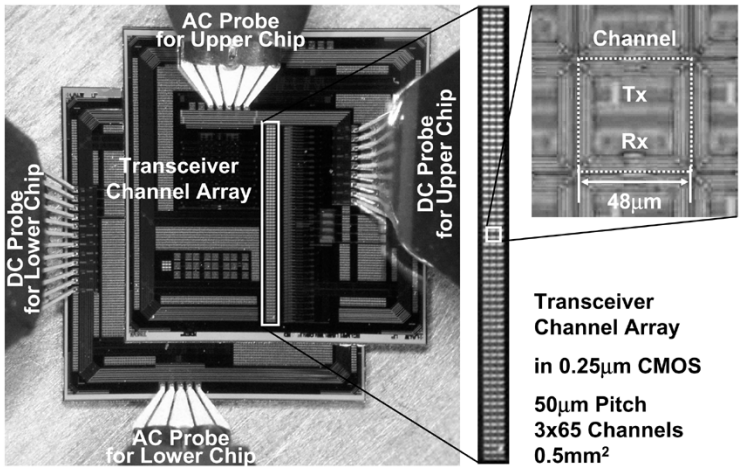

Fig. 2. Microphotograph of stacked test chips and transceiver channel array.

TSV in a face-up or face-down stacked structure while they are required in a face-to-face stacked structure. In a high-performance application where strong power supply is required due to large power dissipation, TSV is necessary to provide power through all stacked chips. However, advanced fine-pitch TSV and at-speed testing are not required just for DC connections so that KGD problem does not occur. Moreover, transmission gain of inductive coupling is enlarged by increasing number of turns of inductors by exploiting an increasing level of metal layers. Reflection or absorption is much smaller since permeability is about the same in semiconductor devices.

We developed the inductive coupled wireless interface, namely, the inductive inter-chip wireless superconnect (WSC). Fig. 1 illustrates the scheme where chips are stacked face-up and inductively coupled by metal inductors. A diagram at the right describes our proposed inductive inter-chip nonreturn-to-zero (NRZ) signaling. A transmitter converts a transition of transmitted data *Txdata* to a bipolar pulse current I_T. Received voltage V_R is induced through inductive coupling at a receiver side. V_R is simply given by $j\omega MI_T$, where M is the mutual inductance between transmitter and receiver inductor. The receiver directly samples the V_R signal with *Rxclk* and recovers data, *Rxdata*. Since V_R is not generated when *Txdata* holds, the receiver's sensitivity has to be controlled and set within appropriate range, so that it can detect signal and ignore noise and crosstalk in V_R. Circuit techniques to solve this problem are presented in [7] and [14]. A data rate of 1.2 Gb/s/channel with 45 mW at 300-μm distance inter-chip communication is reported in [7].

This paper describes a high-bandwidth interface outperforming a 160-Gb/s interface utilizing micro-bump technology [5] by arranging the inductive coupled wireless interfaces in a high-density channel array. The channel pitch is reduced to less than 60 μm for higher density. The aggregate data rate is increased more than 160 Gb/s for higher bandwidth. Over-3-stacked inter-chip communication is demonstrated while micro-bump technology cannot be employed in it. Although finer pitch micro-bumps were reported in [17] and [18], where the bump pitch has been taken down to 10 μm, [5] is the latest implementation of the interface with micro-bump technology for high-bandwidth inter-chip communication including circuits and reliability.

There are three challenges to achieve this goal. 1) Chip thickness $T_{\rm chip}$ should be reduced to increase the number of stacked chips $N_{\rm stack}$. According to a theoretical analysis discussed in [14], it is difficult to make communication distance X longer than the inductor diameter D because of weak coupling and limited area for a transmitter. In the face-to-back stacked structure described in Fig. 1, X is increased by $T_{\rm chip}$ as the number of stacked chips $N_{\rm stack}$ is increased. Since X is limited under the diameter D, maximum $N_{\rm stack}$ is limited under $D/T_{\rm chip}$. Considering the channel pitch of 60 μm, which is almost the same as the inductor diameter D, chip thickness has to be reduced to less than 30 μm to achieve over-3-stacked inter-chip communication. 2) Power reduction is required especially at a transmitter side to achieve parallel connections. A transmitter presented in [7] consumes 42 mW which occupies more than 90% of the transceiver's power dissipation. A new transmitter circuit is necessary and thinning chip thickness, short communication distance, helps to reduce the power also. 3) Crosstalk between channels should be reduced to keep it under the receiver's sensitivity. Crosstalk is analyzed by using a theoretical model discussed in [15], and two-phase TDMA, a crosstalk reduction technique presented in [15], is applied to the channel array for high density channel arrangement.

The rest of this paper is organized as follows. In Section II, implementation and measurement results of the proposed interface will be presented. First, a stack of test chips designed and fabricated in 0.25-μm CMOS technology will be shown. Next, the inductive coupling and transceiver circuit design will be explained with simulation and measurement results. Following an explanation of the transceiver circuit, a channel array structure will be presented with measurement results. Section III will summarize the performance of the proposed interface and compare it with micro-bump technology. Section IV will discuss a scaling scenario and future work of the proposed scheme. Finally, conclusions will be presented in Section V.

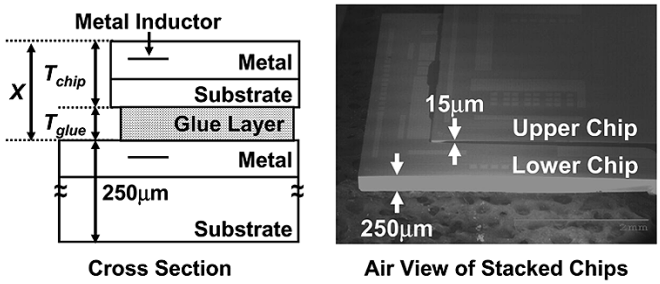

Fig. 3. Cross section and air view of stacked chips.

II. Implementation and Measurement Results

A. Stack of Test Chips

A test chip has been designed and fabricated in a 0.25-μm standard CMOS process. Fig. 2 is a microphotograph of a stack of test chips. 195 transceivers are arranged by 3×65 in 50-μm pitch in a transceiver channel array. In the transceiver, a transmitter (Tx) and a receiver (Rx) circuits are placed under inductors to save layout area. The upper chip is polished, rotated by 180° for probe arrangement, and glued on a lower chip. Test chips are tested in a laboratory room that has no special dust control and electromagnetic interference shields and mounted on a measurement stage which is conductive and connected to ground like a package. Power and ground are provided by DC probes and 1-GHz clock signal, *Clk*, is provided by AC probes. Transmitted data of the center channel in the array, *Txdata*, is given by an external signal source, and received data, *Rxdata*, is monitored through AC probes.

Fig. 3 describes a cross section of the stacked test chips and an air view in an electron microscope picture. The thickness of the upper chip is polished to 10 μm at minimum. Communication distance including glues is 15 μm. The lower chips are not polished. The thickness is 250 μm. Chips are stacked and glued by epoxy resin and aligned with infra red by using on-chip patterns by a top metal layer. Accuracy of the alignment was to less than 1 μm. Based on the measurement results reported in [15], [19], the inductive coupled interface has a good tolerance to misalignment. The misalignment does not matter. Multiple-chip stacking is emulated by changing communication distance between two stacked chips with polishing the upper chips to various thicknesses (10, 20, 30, 40, and 50 μm) prior to the assembly. Several sets of the stacked chips were assembled for demonstrating over-3-stacked inter-chip communications. Measured communication distances are 15, 28, 36, 43, and 59 μm which correspond to 2, 3, 3, 4, and 5 chips stacked.

In order to confirm that thinning and stacking has no effect on transistors, drain characteristics of pMOS transistors in the 10-μm-thickness stacked chip were measured and compared to that in nonpolished bare chip. No effect on the transistor was found in the measurement shown in Fig. 4. It is reported in [16] that substrate thickness can be reduced to 1.7 μm without affecting transistor characteristics. The measurement result is consistent with [16].

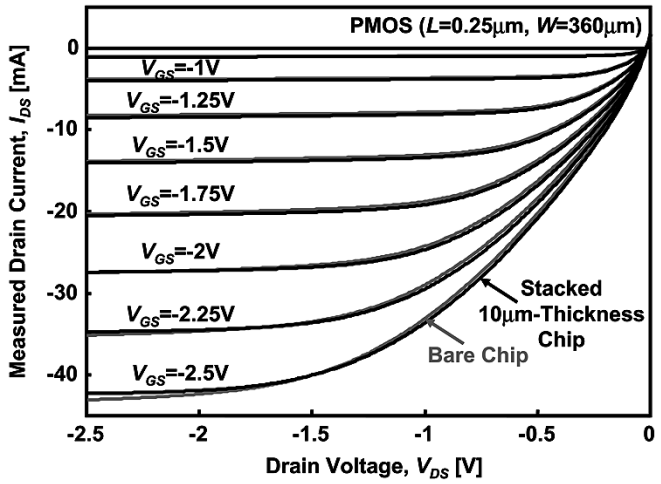

Fig. 4. Measured drain characteristics of pMOS transistor in stacked 10-μm-thickness chip and nonpolished bare chip.

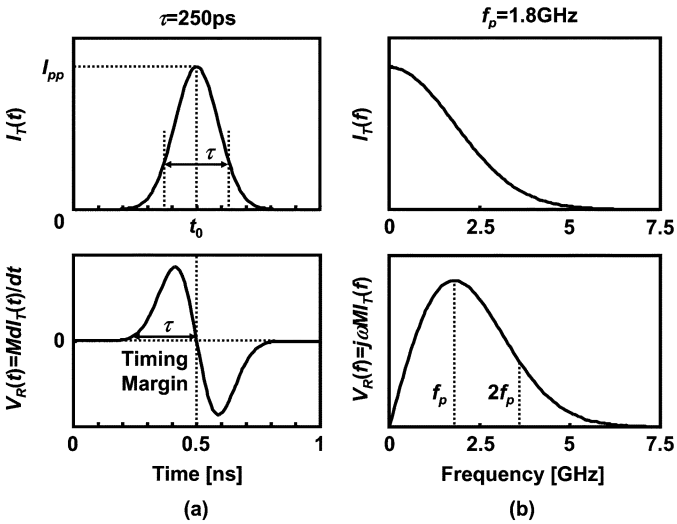

Fig. 5. Characteristics of signals in inductive NRZ signaling (a) in time domain and (b) in frequency domain.

B. Signaling

Inductive inter-chip NRZ signaling was shown in Fig. 1. For general wireless communication, carrier modulation techniques are utilized to obtain high signal-to-noise ratio (SNR) with high-frequency efficiency while sophisticated RF/analog circuits like a mixer, frequency synthesizer, and passive filter are required, which increase power and area. Since transceivers in wireless superconnect communicate in close proximity (several tens of micrometers), much higher SNR can be obtained without carrier modulations. Therefore, a pulse modulation scheme is utilized to reduce circuit complexity. Based on transitions of the transmitted data *Txdata*, pulse current I_T is generated and transmitted through inductive coupling. Received voltage $V_R = j\omega M I_T$ is directly sampled and received data *Rxdata* is recovered.

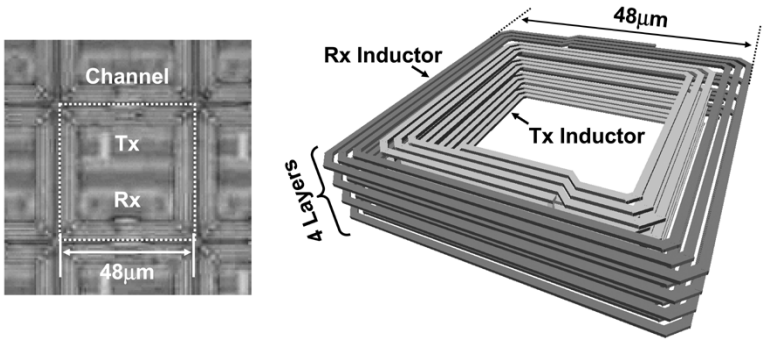

Fig. 6. Microphotograph and layout image of transceiver inductor.

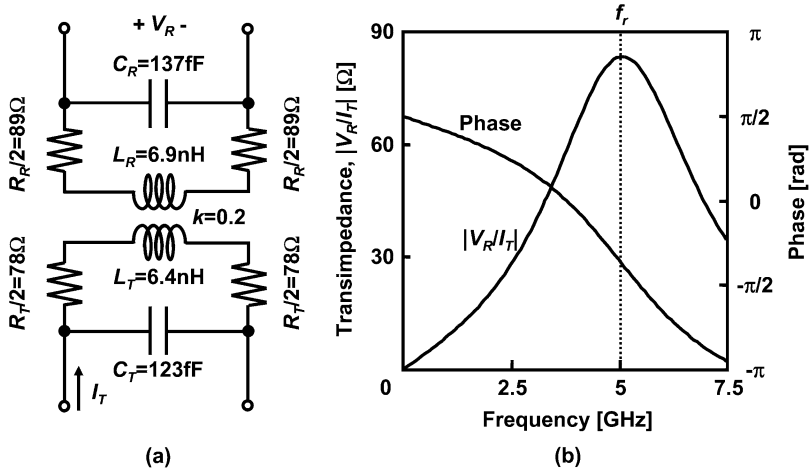

Fig. 7. Model of inductive coupling: (a) equivalent circuit and (b) frequency characteristics.

Fig. 5(a) describes characteristics of the transmitted and received signal in time domain. I_T is modeled as a Gaussian pulse which is given by

$$I_T(t) = I_{\rm pp} \exp\left[-\frac{4(t-t_0)^2}{\tau^2}\right] \tag{1}$$

where $I_{\rm pp}$ is a peak current, t_0 is a time offset, and τ is a pulse width. τ determines the timing margin of the receiver. To obtain the timing margin of over 200 ps, τ is set to 250 ps. In this case, V_R has a pulse width of 500 ps. Therefore, maximum data rate of up to 2 Gb/s/channel can be obtained. However, for the high-density channel arrangement, a two-phase TDMA technique is utilized in a channel array to reduce crosstalk; the data rate becomes 1 Gb/s/channel.

Fig. 5(b) depicts characteristics of the signals in frequency domain. The frequency spectrum of $I_T(t)$ is given by

$$I_T(f) = \frac{\tau I_{\rm pp}}{16\pi} \exp\left(-\frac{\pi^2\tau^2}{4} f^2\right) \exp(-j2\pi f t_0). \tag{2}$$

Essentially, differential operation of inductive coupling is inevitable, therefore $j\omega M I_T(f)$ is the actual frequency spectrum to be analyzed. The frequency spectrum is shown in Fig. 5. The peak frequency (fundamental), f_p, is given by $\sqrt{2}/\pi\tau$. Bandwidth of at least 2 f_p is required for inductive coupling to damp the received signal and diminish inter-symbol interference (ISI).

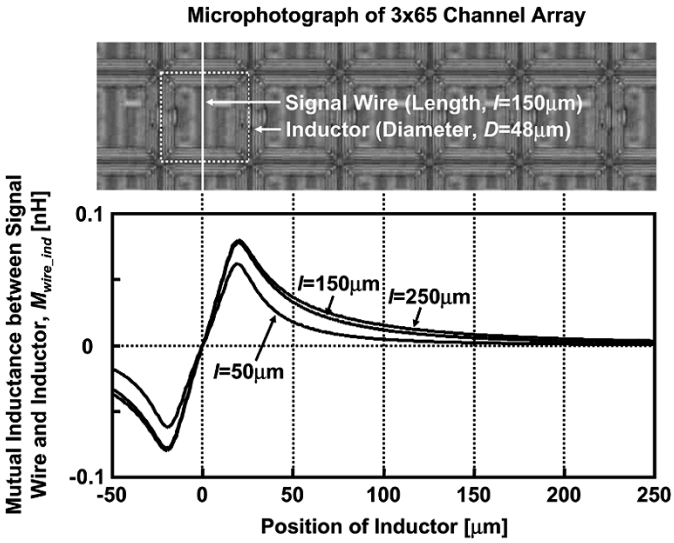

Fig. 8. Calculated interference between signal wire and metal inductor.

C. Metal Inductor

A microphotograph and a layout of a metal inductor for interchip communication are shown in Fig. 6. Based on [14], the transmitter and the receiver have each inductor; the inductor is not shared by the transceiver to avoid ISI and attenuation by bandwidth limitation caused by the transmitter's large output

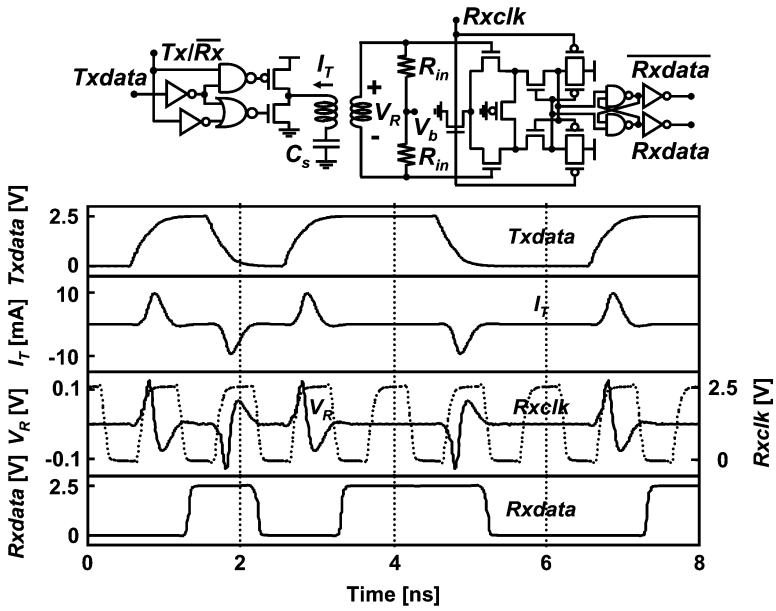

Fig. 9. Transceiver circuit and SPICE simulation results.

capacitance. The transmitter inductor is allocated inside the receiver inductor concentrically as shown in Fig. 6. The diameter of the transceiver inductor is 48 μm. Four metal layers are used and the inductors have three turns in each layer. Self-inductances of the transmitter and receiver inductor, L_T, L_R, are calculated as 6.4 and 6.9 nH, respectively. A simple equivalent circuit is presented in Fig. 7(a). Inductive coupling is modeled by a transformer whose coupling strength is defined as a coupling coefficient, $k = M/\sqrt{L_T L_R}$ which strongly depends on the communication distance between the inductors. The dependence will be shown in Section II-E. The coupling coefficient is 0.2 when the communication distance becomes 15 μm. Parasitic elements like series resistances, R_T, R_R, and parallel capacitances, C_T, C_R, are extracted by a 3-D-field solver. Based on the equivalent circuit, transimpedance of the inductive coupling is given by

$$\frac{V_R}{I_T} = \frac{1}{(1-\omega^2 L_R C_R) + j\omega R_R C_R} \cdot j\omega k\sqrt{L_T L_R} \cdot \frac{1}{(1-\omega^2 L_T C_T) + j\omega R_T C_T}. \quad (3)$$

Frequency characteristics of the inductive coupling are described in Fig. 7(b). Transmitter and receiver inductors are modeled as second-order low-pass filters which have a peaking at self-resonant frequency of $1/2\pi\sqrt{L_T C_T}$ and $1/2\pi\sqrt{L_R C_R}$, respectively. A magnetic coupling is characterized as a differential operator whose gain is $k\sqrt{L_T L_R}(= M)$. In total, inductive coupling behaves as a bandpass filter. The resonant frequency of the inductive coupling, f_r, is almost equal to the self-resonant frequency of the transmitter or receiver inductor. f_r should be higher than $2f_p$ (signal frequency) to suppress ISI. The transceiver inductor is designed for maximizing self-inductance and keeping f_r (= 5 GHz) higher than $2f_p$ (= 3.6 GHz).

In the implemented interface, the transmitter and receiver circuits are placed under the metal inductor. Interference between them does not matter since the transmitter inductor is opened

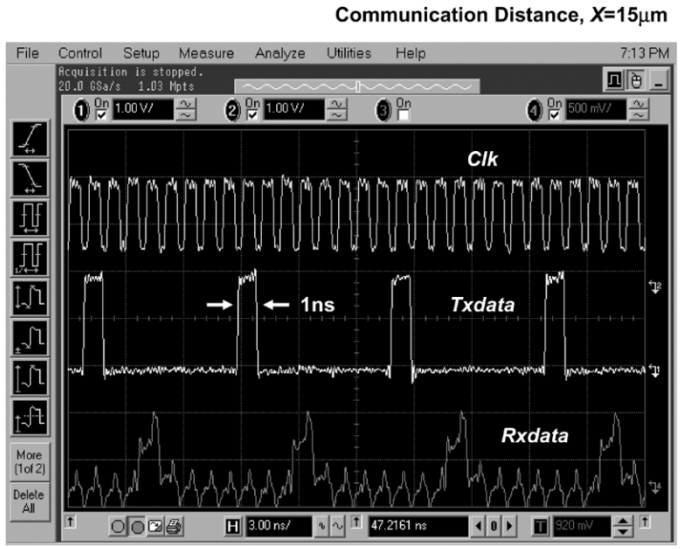

Fig. 10. Measured transmitted and received data at 1 Gb/s.

when the transmitter is not transmitting data by the $Tx/\overline{Rx}$ signal and the receiver has a fully differential structure and a symmetric layout, and the current flow through the receiver is small enough. In addition, long signal wires for data and clock run below the center of the metal inductor. Fig. 8 depicts the calculated position dependence of mutual inductance between the signal wires and the metal inductor, $M_{\mathrm{wire\_ind}}$. The mutual inductance is negligibly small when the wire is located below the center of the metal inductor or the distance between them increases over 100 μm (two channels away) compared to mutual inductance between transmitter and receiver inductor for data communication ($>$0.5 nH). Interference from long wires (l = 150 μm) to the inductor is simulated in SPICE by using the equivalent circuit with $M_{\mathrm{wire\_ind}}$. Since the current flowing in the wire is quite small and the frequency is so high, simulated interference is less than 10-mV-peak voltage, which can be

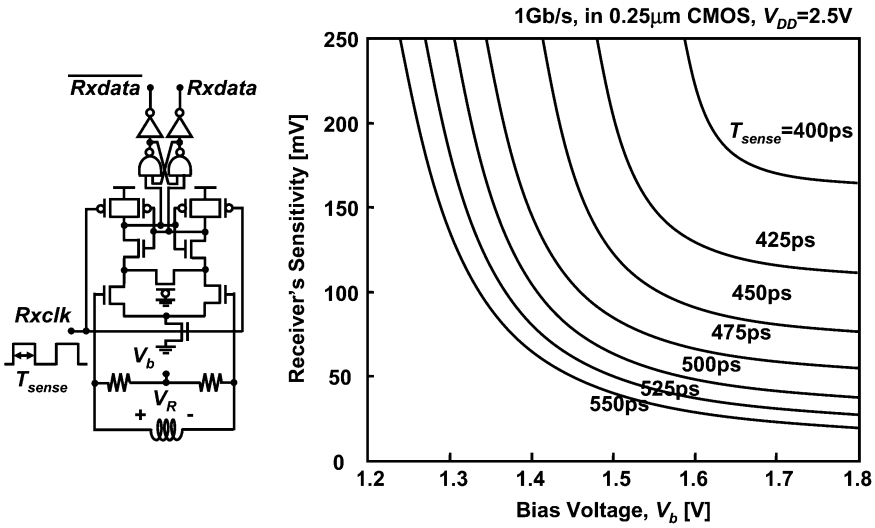

Fig. 11. Receiver's sensitivity control.

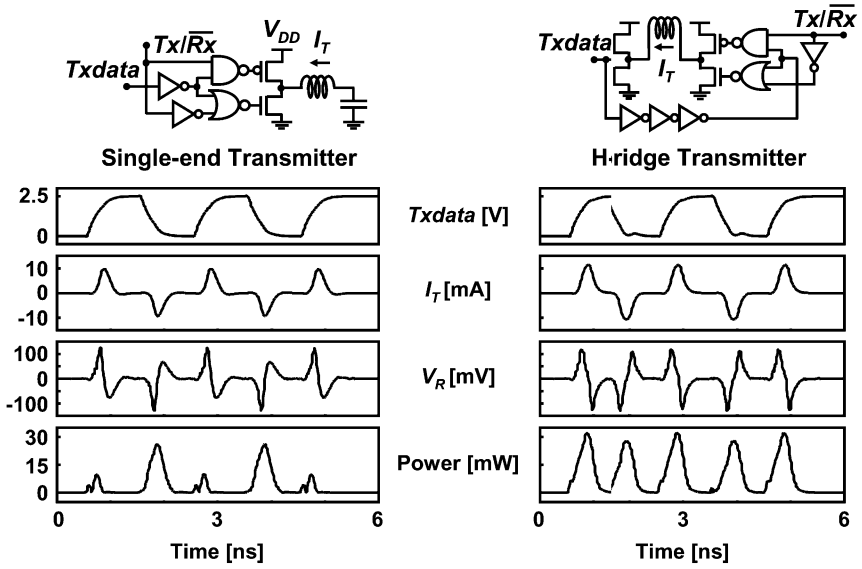

Fig. 12. Comparison between proposed single-end transmitter and conventional h-bridge transmitter.

ignored. Receiver inductors induce no interference because current flow in the receiver inductor is very small (less than 0.1 mA) due to high input impedance of the receiver for voltage sensing. The transmitter inductors generate interference of 60-mV-peak voltage on the wires even in the worst case when all transmitters transmit with the largest power. It is small enough not to affect 2.5-V-swing digital signals.

D. Transceiver Circuit

Fig. 9 describes a transceiver circuit implemented in the test chip with SPICE simulation results shown below. A transmitter is the proposed single-end transmitter which behaves as a simple inverter chain when $Tx/\overline{Rx}$ is high. By using a series capacitor C_s, the bipolar pulse current I_T flows through the transmitter inductor based on a transition of the transmitted data, *Txdata*. The receiver is a sense amplifier with a latch circuit that samples the received voltage V_R with *Rxclk* and recovers received data *Rxdata*. For voltage sensing, input resistances $R_{\rm in}$ should be high (>2 kΩ). Fig. 10 presents measured waveforms of the 1-GHz clock signal *Clk*, 1-Gb/s transmitted data *Txdata*, generated by an external source and provided through AC probes to each chip, and 1-Gb/s received data *Rxdata*, recovered by the receiver circuit through inductive coupling when communication distance $X = 15$ μm. Data rate of up to 1 Gb/s/channel is demonstrated with the transceiver circuit.

The receiver's sensitivity is controlled by a bias voltage V_b and high duration time of a sampling clock $T_{\rm sense}$. Fig. 11 shows that the receiver's sensitivity becomes high when $T_{\rm sense}$ and V_b are increased because longer $T_{\rm sense}$ allows amplification of the V_R signal and higher V_b increases g_m of the differential pair transistors. The receiver's sensitivity can be controlled at the range of around 200 mV.

To reduce power in the transmitter, a single-end transmitter is proposed. Fig. 12 describes a comparison between the single-end transmitter and a conventional h-bridge transmitter proposed in [7] and [14]. The transmitter consumes most of the power at the output inverter which flows pulse current I_T to the transmitter inductor. In the h-bridge transmitter, transmitted

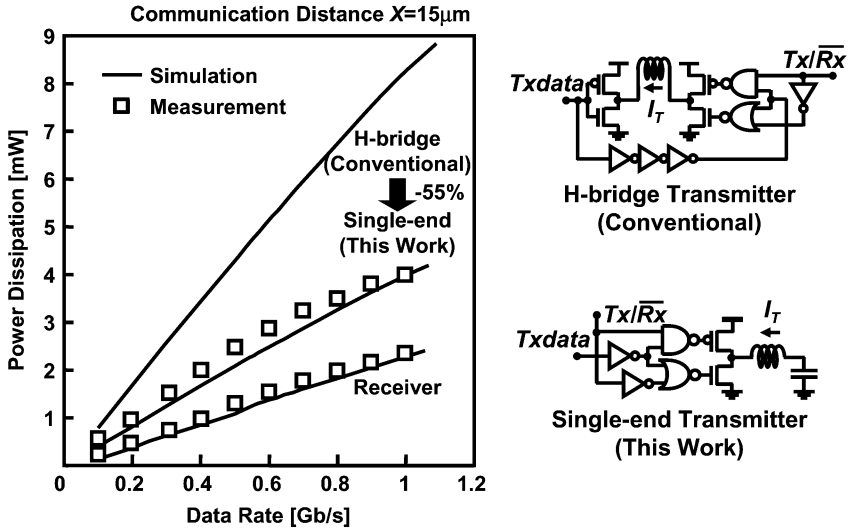

Fig. 13. Measured power dissipation of transceiver circuit.

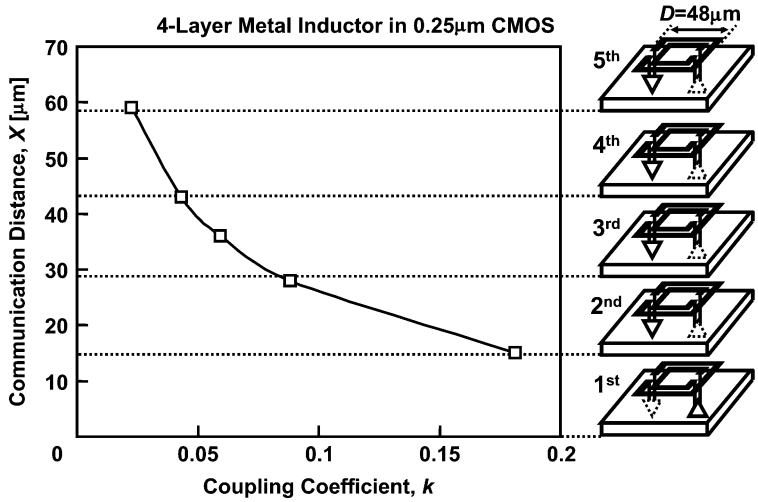

Fig. 14. Calculated coupling coefficient dependence on communication distance.

pulse current I_T becomes short current, therefore it consumes power at every pulse generation. From (1) and Fig. 5, the consumed energy for single pulse generation is approximately given by $\tau I_{\rm pp} V_{\rm DD}$, where $I_{\rm pp}$ is peak current of I_T, $V_{\rm DD}$ is 2.5-V supply voltage, and τ ($= 250$ ps) is given based on the timing margin requirement of the receiver. $I_{\rm pp}$ is determined to induce enough amplitude of the received signal V_R to be detected by the receiver. The V_R amplitude is simply given by $2k\sqrt{L_T L_R} I_{\rm pp}/\tau$. To generate 100-mV amplitude of V_R when $k = 0.2$ ($X = 15$ μm), $I_{\rm pp}$ of 10 mA is required. Then 6.25 pJ of energy is consumed at every pulse generation. In the single-end transmitter, on the other hand, I_T becomes the charge and discharge current of the series capacitor. Since I_T is once charged by the series capacitor and reused for the next opposite pulse generation, the single-end transmitter can generate the I_T signal twice with the same power dissipation of the h-bridge. As a result, at least 50% power reduction would be obtained. Fig. 13 shows the measured power dissipation of the transceiver circuit at the communication distance of 15 μm. The transmitter's power dissipation is reduced by 50% due to I_T difference and 5% due to removal of the delay buffers and one of the output inverters. In total, 55% power reduction is obtained. The single-end transmitter and the receiver dissipate 4 mW and 2.2 mW at 1 Gb/s, respectively.

E. Transmit Power Control

In multiple-stacked inter-chip communication, communication distance differs depending on which layers of stacked chips are communicating. Since the coupling coefficient k (coupling strength) of the inductive coupling strongly depends on the communication distance, received voltage V_R changes at each layer of stacked chips. Fig. 14 shows calculated coupling coefficient between the bottom chip (the first chip) from each layer of stacked chips. k between the first and second chips ($X = 15$ μm) is about 5 times higher than k between the first and fourth chips ($X = 43$ μm). Then V_R is approximately given by

$$V_R = j\omega k \sqrt{L_T L_R} \frac{P_{\rm TX}}{V_{\rm DD}} \tag{4}$$

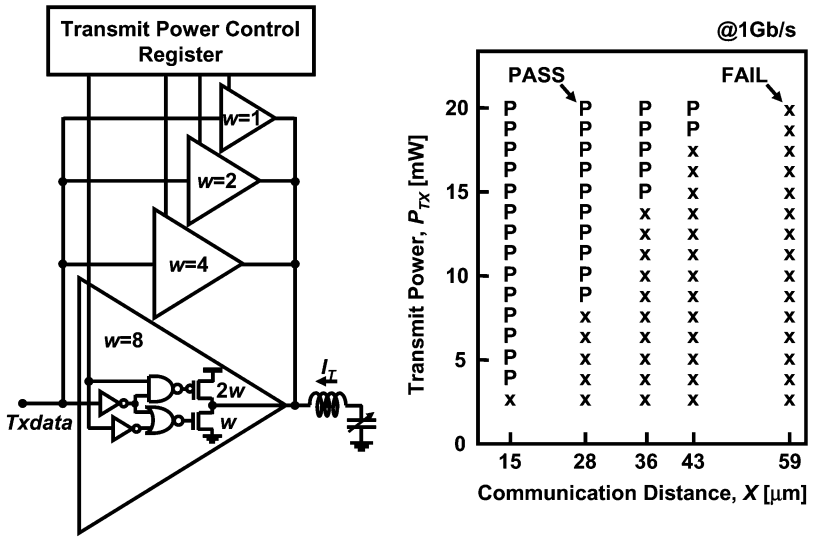

Fig. 15. Transmit power control scheme and measured minimum transmit power dependence of communication distance.

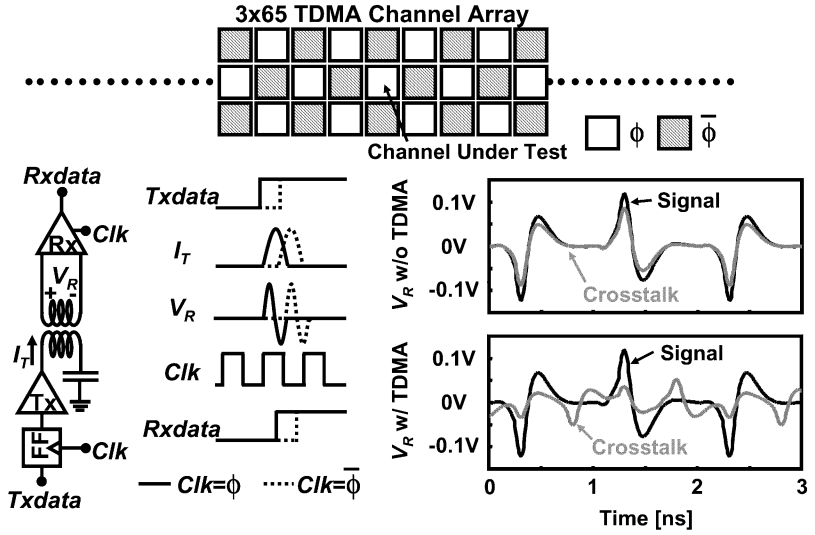

Fig. 16. Channel array utilizing TDMA technique.

where P_{TX} is transmit power and V_{DD} is supply voltage. If a transmitter in the first chip transmits with the same transmit power for all stacked chips, V_R at the second chip becomes about 5 times higher than that at the fourth chip. The transmit power should be reduced when chips are communicating over a short distance.

A transmit power control scheme is presented and applied to the transmitter. Fig. 15 describes the scheme. The transmit power P_{TX} is controlled in 15 levels by a transmit power control register. P_{TX} can be dynamically set to the minimum level required for a given communication distance or depending on which layers of stacked chips are communicating. A measured shmoo plot at the right of Fig. 15 presents the measured minimum transmit power for each communication distance. The required transmit power for communication distances of 15, 28, and 43 μm are 4, 9, and 19 mW, respectively. When the communication distance is reduced to 15 μm from 43 μm, the transmit power can be reduced to 20%.

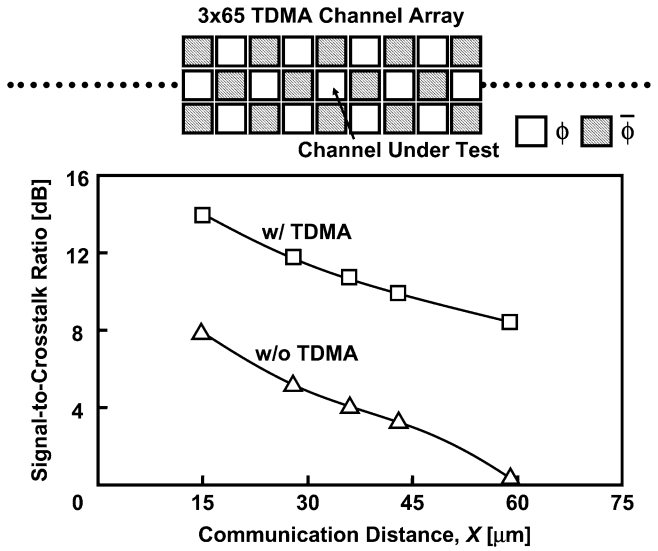

Fig. 17. Relationship between communication distance and signal-to-crosstalk ratio with and without TDMA technique.

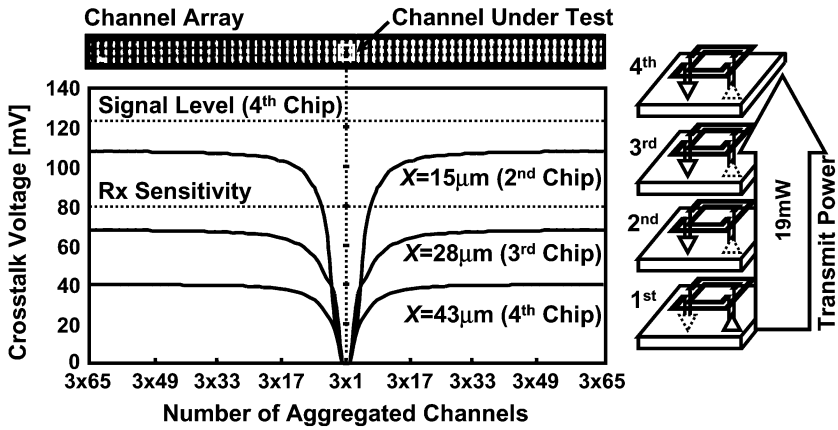

Fig. 18. Calculated total crosstalk at center channel in 3×65 TDMA channel array.

F. Channel Array

In this section, following a presentation of the transceiver circuit implementation, a channel array structure is explained with measurement results. Fig. 16 describes the channel array structure implemented in the test chip. The time division multiple access (TDMA) technique presented in [15] is utilized as a crosstalk reduction technique. Channels are divided in time domain by using dual-edge clocking. One is activated by a positive edge of the clock and the other is activated by the negative edge. These two channels are arranged in a checkerboard pattern in a 3×65 channel array. The signal and total crosstalk in the received voltage V_R at the center channel is calculated. If TDMA is not applied, the crosstalk increases about the same as the signal level. Fig. 17 shows the relationship between communication distance and signal-to-crosstalk ratio of the center channel in the 3×65 channel array with and without TDMA. TDMA reduces crosstalk by more than 50% and keeps it under the receiver's sensitivity for each communication distance. The effectiveness of the TDMA technique is evaluated in detail with a measurement by an embedded voltage detector [15].

Furthermore, the transmit power control is effective for crosstalk reduction in parallel communication. If a transmitter transmits more than necessary power, crosstalk increases in the nearby chips, and hence, the bit error rate (BER) increases. The microphotograph in Fig. 18 shows a top view of the 3×65 channel array. Crosstalk voltage monitored at the center channel in the array is calculated by increasing the number of aggregated channels from the center. If the transmitter transmits with transmit power of 19 mW, the receiver in the fourth chip receives a signal voltage of 120 mV and a crosstalk voltage of around 40 mV. Then, the receiver's sensitivity should be set to around 80 mV to detect the signal and ignore crosstalk with a margin for ignoring on-chip interference or noise. At the same time, the receiver in the second chip receives a crosstalk voltage of over 80 mV. As a result, the receiver detects crosstalk and erroneously operates when the number of aggregated channels is increased, therefore channels cannot be increased anymore and bandwidth is significantly limited. The transmit power control scheme solves this problem by reducing crosstalk when the communication distance is short.

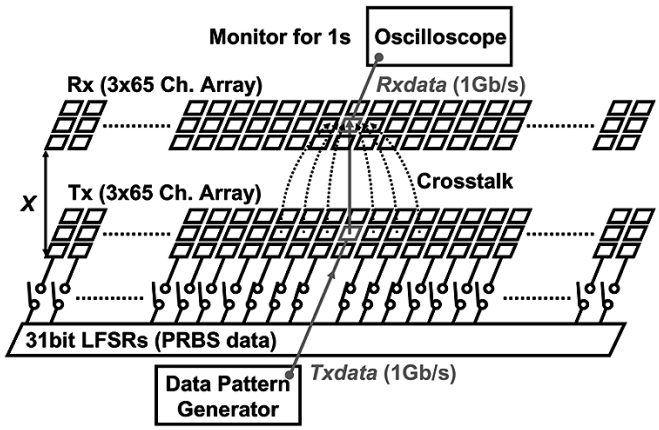

Fig. 19. Experimental setup of inter-chip communication by channel array.

The channel array with the transmit power control scheme is evaluated in an experimental setup described in Fig. 19. The center channel of the channel array in the lower chip transmits 1-Gb/s *Txdata* generated by an external data pattern generator and the other 194 surrounding channels transmit $2^{31}-1$ pseudo-random binary sequence (PRBS) data generated by four on-chip linear feedback shift registers (LFSRs). The number of activated channels is digitally selected. The received data, *Rxdata*, is monitored through a center channel in the upper chip for one second with increasing number of aggregated channels by three channels (one line) from the center. These surrounding channels become a crosstalk noise source for the receiving center channel. When errors are found in *Rxdata*, channels cannot be increased anymore, therefore the maximum number of aggregated channels can be measured with this experiment.

Fig. 20 presents the measurement results. PASS (denoted by P) means that there is no error in the received data for one second (BER $<10^{-9}$). PASS and FAIL (denoted by x) are plotted by increasing the number of aggregated channels by 3 from the center. If transmit power is not controlled, the crosstalk level exceeds the receiver's sensitivity in the second chip. As a result, the center channel erroneously operates when the number of channels exceeds 3×13 channels. Therefore, the aggregate data rate is limited to only 39 Gb/s. On the other hand, if transmit power is controlled depending on communication distance, the crosstalk is reduced and the aggregate data rate is increased to 195 Gb/s for all communication distance.

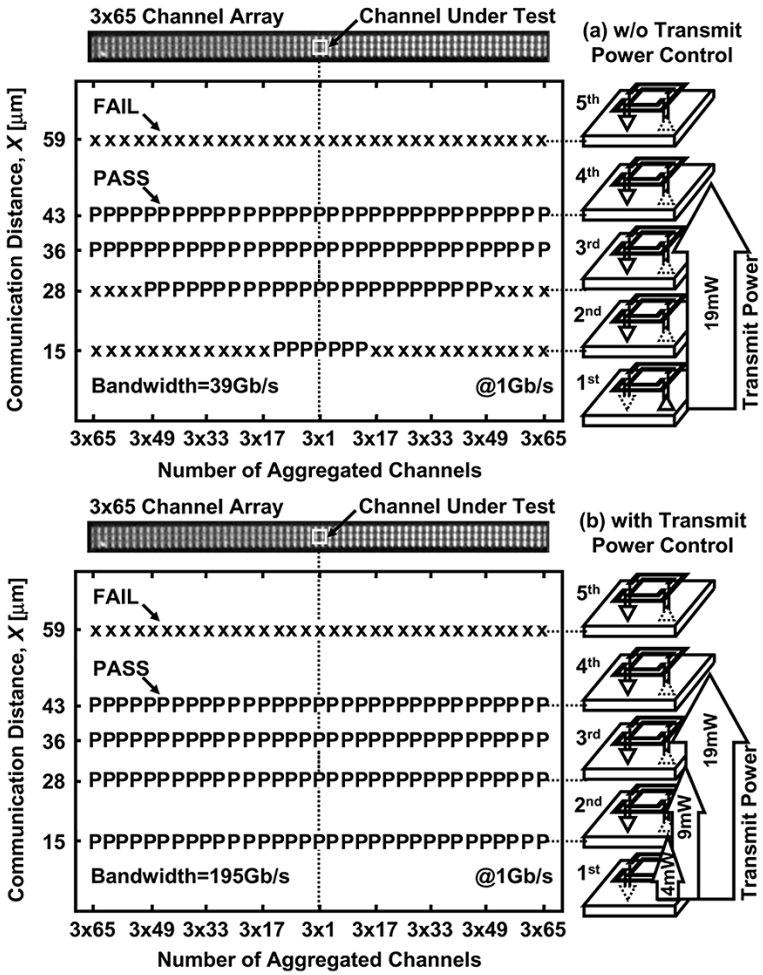

Fig. 20. Measured shmoo plot on number of aggregated channels and communication distance, (a) without and (b) with transmit power control.

III. Performance Summary and Comparison

Table I summarizes the performance of the proposed inductive coupled interface and compares it with the interface using micro-bump technology [5]. Aggregate data rate of 195 Gb/s is achieved. The aggregate data rate is increased by 35 Gb/s. It can communicate at 195 Gb/s between up to 4-stacked chips whether they are face-up or face-down, while the micro-bump can be applied to only two face-to-face chips. The chip thickness is reduced to 10 μm; the communication distance between two chips including glues is 15 μm. Depending on the communication distance, the transmit power is controlled to reduce both power dissipation and crosstalk. Compared to the micro-bump interface, the total area is reduced by a factor of 9 and the channel pitch is reduced by 10 μm even in a less advanced technology.

IV. Discussion

A. Scaling Scenario

Based on the measurement and analysis in [15], increasing the horizontal distance will attenuate the crosstalk more rapidly than increasing the number of channels. Crosstalk is rapidly saturated in the 3×65 channel array as shown in Fig. 13, therefore BER will hardly increase when the channel array is larger than 3×65. Aggregated data rate of 390 Gb/s/mm ^{2} is quite possible in 0.25-μm CMOS.

In addition, it is reported in [16] that substrate thickness is reduced to 1.7 μm without affecting transistor characteristics. Based on a simulation study using 90-nm BSIM model in SPICE simulation, if the communication distance is reduced to 10 μm (further 5 μm reduction), an aggregate data rate of 1.5 Tb/s/mm ^{2} can be achieved with a power dissipation of 5 W by arranging 1500 transceiver channels in 25-μm pitch.

B. Multi-Drop Bus Connections

Signals for the transmit power control or other global control signal in a system should be transmitted and received by multi-drop bus connections. For the multi-drop bus communications, the transmit power should be large enough to communicate with a chip which is at the farthest distance; transmit power control cannot be utilized. The receiver sensitivity should be controlled in each chip or the space between channels should be enlarged to reduce the crosstalk, or the channel for the bus connections should be separated from the high-density channel array. This is a drawback of the inductive NRZ signaling. Bi-phase modulation (BPM) signaling can solve this problem. A transmitter in the BPM signaling generates positive and negative pulse currents whenever it transmits data as 1 and 0, respectively, so that a receiver always receives induced voltage V_R at the sampling.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This Work			Ref. [5]
Aggregate Data Rate	195Gb/s			160Gb/s
Number of Chips that Communicate	2 Chips	3 Chips	4 Chips	2 Chips (Face-to-Face Only)
Communication Distance	15μm	30μm	45μm	No Data
Total Power Dissipation	1.2W	2.2W	4.1W	No Data
Total Area	0.5mm^2			4.5mm^2
Channel Pitch	50μm			60μm
Process	CMOS 0.25μm			CMOS 0.15μm
Interconnect	Wireless (Inductive Coupling)			Wired (Micro Bump)

[5] T.Ezaki, *et al.* (ISSCC'04)

C. Synchronization

Our proposed inductive inter-chip NRZ signaling, shown in Fig. 1, is a pulse modulation technique which requires an accurate synchronization system. In our measurement, timing is controlled by an external source. The synchronization functions, such as source synchronous or clock data recovery (CDR), will be future work using this scheme.

D. Electromagnetic Interference

One of the issues of wireless interfaces may be electromagnetic interference (EMI) between circuits and interfaces. Interference generated by a power-consuming circuit, like a CPU, may degrade the signal between wireless channels and the interface may destroy data in a memory. Both of them would be reduced by a differential structure.

V. CONCLUSION

A 195-Gb/s inductive coupled wireless interface has been proposed. 195 channels which achieve data rate of up to 1 Gb/s/channel are arranged in 50-μm pitch in a 3×65 TDMA channel array. By thinning chip thickness to 10 μm, the interface communicates at distance of 15 μm at minimum and 43 μm at maximum which corresponds to 4-stacked inter-chip communication. A low-power single-end transmitter for 55% transmitter power reduction has been proposed and evaluated with measurements. In addition, a transmit power control scheme has been proposed not only for power reduction but also for crosstalk reduction. Based on communication distance, power dissipation is reduced to 1.2 W at 15 μm. The transmit power control scheme reduces crosstalk and increases bandwidth by 5 times at 15 μm. The proposed interface has been compared with the interface using micro-bump technology. Aggregated data rate is increased by 35 Gb/s, channel pitch is reduced by 10 μm even in a less advanced technology, and total area is reduced by a factor of 9.

ACKNOWLEDGMENT

The VLSI chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC), University of Tokyo, in collaboration with MOSIS and Taiwan Semiconductor Manufacturing Company (TSMC). The authors are grateful to M. Tago, M. Fukaishi, and Y. Nakagawa with NEC Corporation for their assistance in measurement.

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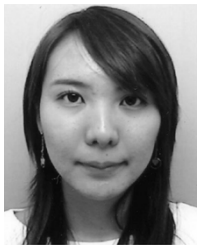

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